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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

KAMNIZ HAYAT-DAWOODI

Serial No. 09/873,057 (TI-29619)

Filed June 2, 2001

For: INTEGRATED CIRCUIT LEADFRAMES PATTERNED FOR MEASURING THE ACCURATE AMPLITUDE OF CHANGING CURRENTS

Art Unit 2829

Examiner Russell Marc Kobert

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3-1-04

JAY H. CANTOR

Sir:

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences.

STATUS OF CLAIMS

This is an appeal of claims 1 to 5 and 7 to 9, all of the rejected claims. No claims have been allowed and claims 6 and 10 to 21 have been withdrawn from consideration. Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

An amendment was not filed after final rejection.

SUMMARY OF INVENTION

The invention relates to a metallic leadframe structure for use with a semiconductor chip intended for operation in a changing magnetic field. The leadframe includes a chip mount pad (201, 301, 401, 501) having at least one slit (205, 302, 402, 502) penetrating the entire thickness of the pad and substantially traversing the area of the pad from one edge to the opposite edge. The slit is sufficiently wide to interrupt electron flow in the pad plane, but sufficiently thin to significantly reduce thermal conduction in a direction normal to the pad plane, the slit being thereby operable to disrupt eddy currents induced in the pad by the changing magnetic field. The slit preferably has a width from about 0.01 to 0.5 mm and preferably is a sheet-like starting configuration having a thickness in the range from about 100 to 300 μm. The sheet-like starting configuration is preferably selected from a group of metals consisting of copper, copper alloy, brass, aluminum, iron-nickel alloy, and invar. The pad can have an area larger than the chip intended for mounting.

A second embodiment includes the leadframe structure having a semiconductor chip thereon, the chip having an integrated circuit including a Hall device.

A third embodiment includes a plurality of slits (Figs. 4 and 5) in a configuration operable to suppress eddy currents induced in said pad by said changing magnetic field, each slit sufficiently wide to interrupt electron flow in the pad plane, but sufficiently narrow to significantly reduce thermal conduction in a direction normal to the pad plane. The plurality of slits can be configured approximately parallel or approximately star-burst-like, or in any pattern

suitable for suppressing the origin of eddy currents, while preserving the mechanical stability and thermal conduction of said leadframe.

ISSUES

The issues on appeal are as follows:

1. Whether claims 1 to 5 and 7 to 9 are definite under 35 U.S.C. 112, second paragraph.

2. Whether claims 1, 5, 6 and 9 are anticipated by Manabe (U.S. 4,797,726) under 35 U.S.C. 102(b).

3. Whether claims 2 and 3 are patentable over Manabe under 35 U.S.C. 103(a).

4. Whether claim 4 is patentable over Manabe in view of Brown (U.S. 4,918,511) under 35 U.S.C. 103(a).

GROUPING OF CLAIMS

The dependent claims stand or fall with the claims from which they depend.

ARGUMENT

ISSUE 1

Claims 1 to 5 and 7 to 9 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite. The rejection is without merit.

The Examiner states that the feature of the claims relating to the fact that "a slit or plurality of slits wide enough to interrupt electron flow but not wide enough to significantly reduce thermal conduction in a leadframe structure" is not a limitation in the structure of claims 1 and 8. This allegation is completely without basis and defies the facts of record.

Claims 1 and 8 specifically require a slit (claim 1) or a plurality of slits (claim 8) in the chip mount pad which penetrates the entire thickness of the chip mount pad. This alone is a

structural limitation. Claims 1 and 8 further require that the slits have a width which is sufficient to prevent eddy current)claimed as electron flow), yet not sufficiently wide to significantly reduce thermal conduction in a direction normal to the pad plane. This is a specific limitation on the width of the slits, requiring that the slits be sufficiently wide to prevent electron flow or eddy currents, yet not be so wide as to substantially affect the ability for the pad to thermally conduct heat from the chip or any other heat producing member thereon. It is quite clear that the slits could be configured to be so large as to leave only a very small amount of pad. While such a configuration would interrupt electron flow in the pad plane, it also would not provide an effective heat sink as required by claims 1 and 8. It follows that such a configuration is specifically eliminated from these claims. The amount of pad remaining must be sufficient to provide sufficient heat sink properties for the intended purpose. It follows that claims 1 and 8 are definite.

Claim 18 sets forth the above in broader language by stating that "providing a metallic leadframe having a chip mount pad reducing or eliminating eddy currents in the vicinity of the Hall structure. Again, while the slits are not specifically required in this claim, the pad is still required to contain a mechanism of some sort that eliminates eddy currents at least in the vicinity of the Hall structure. This is a specific limitation of the chip mount pad and is definite.

As stated during prosecution of the subject application, the precise width will be dependent upon a number of factors, including the size of the chip mount pad, the magnitude of the current and magnetic field being measured, the heat dissipated by the chip, and so forth, a fact which would be apparent to one skilled in the art. Given the variability inherent in such a situation, applicant respectfully submits that the claims particularly point out and distinctly claim the subject matter to the extent that the subject matter allows. Therefore, the Examiner's decision to not consider the pertinent claim language as further limiting the structure referred to in Claims 1 and 8 is also in error.

ISSUE 2

Claims 1, 5, 8, and 9 stand rejected under 35 U.S.C. 102(b) as being anticipated by Manabe (U.S. Patent No. 4,797,726). The rejection is without merit.

To begin with,, Manabe has nothing whatsoever to do with the problem involved or the solution thereto. The environment in which the leadframe of the subject invention is to be used is not only set forth in the specification, but is also included in the claims by stating the that the semiconductor chip is intended for operation in a changing magnetic field.

Furthermore, claims 1 and 8 include the feature of a "slit wide enough to interrupt electron flow in the pad plane, but not wide enough to significantly reduce thermal conduction in a direction normal to said pad plane." Manabe nowhere teach or even remotely suggests a chip mount pad having such properties. As understood by the undersigned, an with reference to Fig. 3 of Manabe, there is a chip fixing plate 2, the same as is shown in Fig. 1 holding the chip 1, with four supporting plates (6, 7, 8, 9) on the fixing plate 2 separated from each other by four deformable plates (10, 11, 12, 13). The supporting plates are integral with the deformable plates (col. 2, lines 48 to 50). It follows that, not only does Manabe fail to have slits for any purpose in the chip mount pad, but, in addition, the supporting plates are integral with the deformable plates, thereby making the entire structure of Manabe a continuous electrically conducting structure. It follows that Manabe does not and cannot "interrupt electron flow in the pad plane".

In is again noted that Manabe says nothing about electron flow or thermal conduction before and after the formation of the plates separated by a gap. Since Manabe is deficient in anticipating all of the features of the claims, Applicant respectfully submits that the rejection is improper and is without merit.

Claims 5 and 9 depend from Claims 1 and 8 and are therefore allowable over Manabe by virtue of their dependence from a patentable base claim. In addition, Claim 9 states that the slits are configured such that the mechanical stability and thermal conduction of the leadframe is preserved. Manabe teaches away from the mechanical stability limitation. In Figures 4A-4C of Manabe, it is apparent that the gap in the leadframe increases, and that the bend angle of the bent potion of the readily deformable plate 10 changes during heating. Thus, Manabe is not configured in such a way that the mechanical stability of the leadframe is preserved. Therefore, Applicant respectfully submits that the rejection is without merit.

ISSUE 3

Claims 2 and 3 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Manabe. The rejection is without merit.

Claims 2 and 3 depend from Claim 1. Accordingly, the arguments presented above with reference to claim 1 apply as well to these claims.

ISSUE 4

Claim 4 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Manabe and further in view of Brown (U.S. Patent No. 4,918,511). The rejection is without merit.

Claim 4 depends from claim 3 and therefore defines patentably over the applied references for at least the reasons presented above with reference to claim 3 since Brown fails to overcome the deficiencies in Manabe as set forth above.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,

Jay M. Cantor
Reg. No. 19906
(301) 424-0355

APPENDIX

The claims on appeal read as follows:

1. A metallic leadframe structure for use with a semiconductor chip intended for operation in a changing magnetic field, comprising:

a chip mount pad having at least one slit penetrating the whole thickness of said pad and substantially traversing the area of said pad from one edge to the opposite edge; and

said slit wide enough to interrupt electron flow in the pad plane, but not wide enough to significantly reduce thermal conduction in a direction normal to said pad plane, whereby said slit is operable to disrupt eddy currents induced in said pad by said changing magnetic field.

2. The leadframe according to Claim 1 wherein said slit has a width from about 0.01 to 0.5 mm.

3. The leadframe according to Claim 1 wherein said structure comprises a sheet-like starting configuration having a thickness in the range from about 100 to 300 μm.

4. The leadframe according to Claim 3 wherein said sheet-like starting configuration is selected from a group of metals consisting of copper, copper alloy, brass, aluminum, iron-nickel alloy, and invar.

5. The leadframe according to Claim 1 wherein said pad has an area larger than said chip intended for mounting.

7. A packaged semiconductor device including a ~~The~~ leadframe according to Claim 1, said device further comprising a chip wherein said chip has an integrated circuit including a Hall device.

8. A metallic leadframe structure for use with a semiconductor chip intended for operation in a changing magnetic field, comprising:

a chip mount pad having a plurality of slits in a configuration operable to suppress eddy currents induced in said pad by said changing magnetic field;

each of said slits wide enough to interrupt electron flow in the pad plane, but not wide enough to significantly reduce thermal conduction in a direction normal to said pad plane.

9. The leadframe according to Claim 8 wherein said plurality of slits is configured approximately parallel or approximately star-burst-like, or in any pattern suitable for suppressing the origin of eddy currents, while preserving the mechanical stability and thermal conduction of said leadframe.